Si8285/86 Data Sheet

SiC FET-Ready ISODrivers with System Safety Features

The Si828x (Si8285 and Si8286) are isolated, high current gate drivers with integrated system safety and feedback functions. The devices are ideal for driving Silicon Carbide (SiC) FETs, power MOSFETs, and IGBTs used in a wide variety of inverter and motor control applications. The Si8285 and Si8286 isolated gate drivers utilize Skyworks' proprietary silicon isolation technology, supporting up to 5.0 kVrms withstand voltage per UL1577. This technology enables higher performance, reduced variation with temperature and age, tighter part-to-part matching, and superior common-mode rejection compared to other isolated gate driver technologies.

The input to the device is a complementary digital input that can be utilized in several configurations. The input side of the isolation also has several control and feedback digital signals. The controller to the device receives information about the driver side power state (Si8285) and fault state of the device and recovers the device from fault through an active-low reset pin.

On the output side, the Si8285 provides separate pull-up and pull-down pins for the gate. The Si8286 has a single pin for both functions. A dedicated DSAT pin detects a desaturation condition and immediately shuts down the driver in a controlled manner using soft shutdown. The Si8285 device also integrates a Miller clamp to assure a strong turn-off of the power switch.

Automotive Grade is available. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Industrial Applications

- SiC/IGBT/ MOSFET gate drives
- Industrial and renewable energy inverters
- AC, Brushless, and DC motor controls
- Variable-speed motor controllers
- Isolated switch mode power supplies

Automotive Applications

- Hybrid electric and electric vehicles
- Traction inverters
- On-board chargers
- Inductive chargers
- DC-DC converters

Safety Regulatory Approvals

- UL 1577 recognized: 5000 V_{RMS} for 1 minute
- CSA approval: IEC 62368-1 (reinforced insulation)
- VDE certification: IEC 60747-17 (basic, pending), 62368-1 (reinforced insulation)
- CQC certification approval: GB4943.1-2011 (reinforced insulation)

KEY FEATURES

- System Safety Features
  - DESAT detection
  - FAULT feedback
  - Undervoltage Lock Out (UVLO) including 13 and 15 V for SiC FET
  - Soft shutdown on fault condition
  - Ultra-fast short circuit protection << 1 µs
  - Robust reference design for current boost, DESAT adjustment, soft shutdown tuning, and external Miller clamp transistor
- High-performance isolation technology
- High CMTI 125 kV/µs
- 30 V driver-side supply voltage
- Integrated Miller clamp (Si8285 only)
- Power ready pin (Si8285 only)
- Complementary driver control input
- Si8286 pin-out compatible with HCPL-316J
- Compact package: 16-pin wide-body SOIC
- Automotive-grade OPNs available
  - PPAP documentation support
  - IMDS and CAMDS listing support
  - AEC-Q100 Qualified
- Temp range: –40 to 125 °C

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1. Si8285/86 Ordering Guide

Industrial and Automotive Grade OPNs

Industrial-grade devices (part numbers having an “-I” in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers having an “-A” in their suffix) are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listing. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps.

Table 1.1. Si8285/86 Ordering Guide

Ordering Part Number (OPN)	A-Grade OPN	Ordering Options			Package
		Pin Compatibility	UVLO (V)	Isolation Rating (kVrms)	
Si8285BC-IS	Si8285BC-AS	—	9	3.75	WB SOIC-16
Si8285CC-IS	Si8285CC-AS	—	12	3.75	WB SOIC-16
Si8285DC-IS	Si8285DC-AS	—	13	3.75	WB SOIC-16
Si8285EC-IS	Si8285EC-AS	—	15	3.75	WB SOIC-16
Si8286BC-IS	Si8286BC-AS	HCPL-316J	9	3.75	WB SOIC-16
Si8286CC-IS	Si8286CC-AS	HCPL-316J	12	3.75	WB SOIC-16
Si8286DC-IS	Si8286DC-AS	HCPL-316J	13	3.75	WB SOIC-16
Si8286EC-IS	Si8286EC-AS	HCPL-316J	15	3.75	WB SOIC-16
Si8285BD-IS	Si8285BD-AS	—	9	5	WB SOIC-16
Si8285CD-IS	Si8285CD-AS	—	12	5	WB SOIC-16
Si8285DD-IS	Si8285DD-AS	—	13	5	WB SOIC-16
Si8285ED-IS	Si8285ED-AS	—	15	5	WB SOIC-16
Si8286BD-IS	Si8286BD-AS	HCPL-316J	9	5	WB SOIC-16
Si8286CD-IS	Si8286CD-AS	HCPL-316J	12	5	WB SOIC-16
Si8286DD-IS	Si8286DD-AS	HCPL-316J	13	5	WB SOIC-16
Si8286ED-IS	Si8286ED-AS	HCPL-316J	15	5	WB SOIC-16

Note:

1. Add an "R" at the end of the Part Number to denote Tape and Reel option.
2. All packages are RoHS-compliant with peak solder reflow temperatures of 260° C according to the JEDEC industry standard classifications.
3. A-grade OPNs are AEC-Q100 qualified.
4. “Si” and “SI” are used interchangeably.
5. Automotive-Grade devices (with an "–A" suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade (with a "–I" suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
6. In the top markings of each device, the Manufacturing Code represented by either “RTTTTT” or “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive-Grade.

2. Product Overview

2.1 Isolation Channel Description

The operation of a Si8285 or Si8286 channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si828x channel is shown in the figure below.

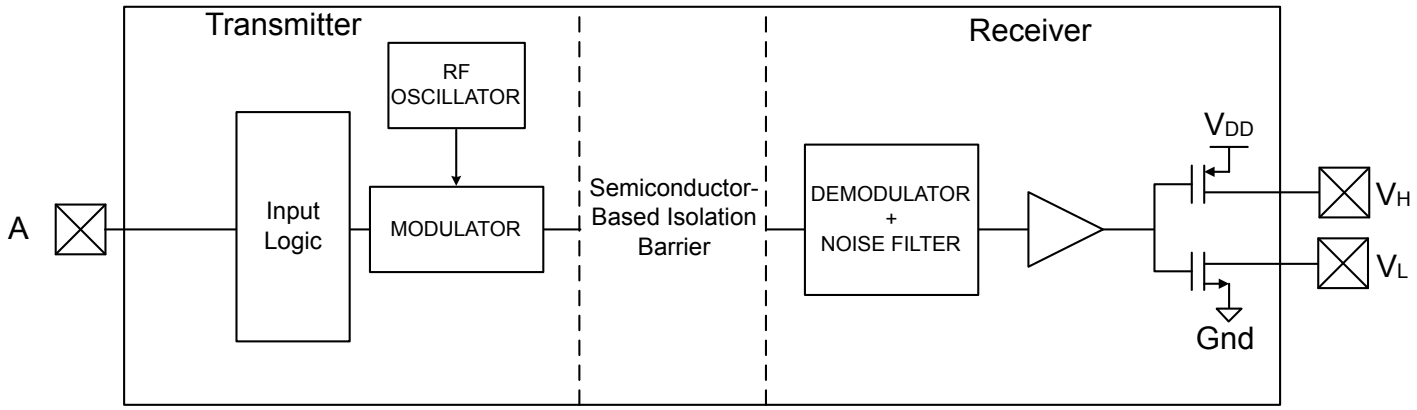


Figure 2.1. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields.

2.2 Device Behavior

The following tables show the truth tables for the Si8285 and Si8286.

Table 2.1. Si8285 Truth Table

IN+	IN–	VDDA State	VDDB–VMID State	Desaturation State	VH	VL	RDY	FLTb
H	H	Powered	Powered	Undetected	Hi-Z	Pull-down	H	H
H	L	Powered	Powered	Undetected	Pull-up	Hi-Z	H	H
L	X	Powered	Powered	Undetected	Hi-Z	Pull-down	H	H
X	X	Powered	Unpowered	—	—	—	L	H
X	X	Powered	Powered	Detected	Hi-Z	Pull-down[1]	H	L

Note:
1. Driver state after soft shutdown.
2. This table is valid if RSTb is deactivated (high). For further information please refer to **Reset (RSTb) Pin description**.

Table 2.2. Si8286 Truth Table

IN+	IN–	VDDA State	VDDB–VMID State	Desaturation State	VO	FLTb
H	H	Powered	Powered	Undetected	Low	H
H	L	Powered	Powered	Undetected	High	H
L	X	Powered	Powered	Undetected	Low	H
X	X	Powered	Powered	Detected	Low[1]	L

Note:
1. Driver state after soft shutdown.

2.3 Main Features

Input

The IN+ and IN– inputs to the Si828x devices act as a complementary pair. If IN– is held low, then IN+ will act as an active-high input for driver control. Alternatively, if IN+ is held high, then IN– can be used as an active-low input for driver control. When IN– is used as the control signal, taking IN+ low will hold the output driver low.

Output

The Si8285 and Si8286 devices are different in how the driver output is presented. The Si8285 has separate pins for gate drive high (VH) and gate drive low (VL). This makes it simple to use different gate resistors to control IGBT VCE or SiC FET VDS rise and fall time. The Si8286 has both actions combined in the single VO pin. A weak internal pulldown resistor of about 200 kΩ is provided to ensure that the driver output defaults to low if power on the secondary side is interrupted.

Desaturation Detection

The Si828x provides sufficient voltage and current to drive and keep the SiC FET or IGBT in saturation during on time to minimize power dissipation and maintain high efficiency operation. However, abnormal load conditions can force the SiC FET or IGBT out of saturation and cause permanent damage to the switch.

To protect the SiC FET or IGBT during abnormal load conditions, the Si828x detects a switch desaturation condition, shuts down the driver upon detecting a fault, and provides a fault indication to the controller. These integrated features provide desaturation protection with minimum external BOM cost.

Soft Shutdown

To avoid excessive dV/dt on the SiC FET or IGBT during fault shut down, the Si828x implements a soft shut down feature to discharge the switch's gate slowly.

Fault (FLTb) Pin

FLTb is an open-drain type output. A pull-up resistor takes the pin high. When the desaturation condition is detected, the Si828x indicates the fault by bringing the FLTb pin low. FLTb stays low until the controller resets the desaturation fault by driving the RSTb pin low.

Note: This FLTb behavior is only valid when, prior to the desaturation condition being detected, there were no undervoltage lockout (UVLO) conditions.

Reset (RSTb) Pin

The RSTb pin is active low and is used to clear the desaturation condition and bring the Si828x driver back to an operational state. Even though IN+ and IN- may be toggling, the driver output will not change state until the fault condition has been reset. Both RSTb and FLTb should be high before resuming operation.

Undervoltage Lockout (UVLO)

The UVLO circuit unconditionally drives VL low when VDDB is below the lockout threshold. The Si828x is maintained in UVLO until VDDB rises above $VDDB_{UV+}$. During power down, the Si828x enters UVLO when VDDB falls below the UVLO threshold minus hysteresis (i.e., $VDDB \leq VDDB_{UV+} - VDDB_{HYS}$).

Note: UVLO voltage is evaluated between VDDB and VMID. The VSSB pin should be shorted to VMID if a negative gate bias is not utilized.

Ready (RDY) Pin (Si8285 Only)

The ready pin indicates to the controller that power is available on both sides of the isolation, i.e., at VDDA and VDDB. RDY goes high when both the primary side and secondary side UVLO circuits are disengaged. If the UVLO conditions are detected on either side of the isolation barrier, the ready pin will return low. RDY is a push-pull output pin and can be floated if not used. The recommendation is to put a 10kΩ pulldown to ground on this pin to help prevent a false "Ready" indication when power supplies are below operating conditions (VDDA UVLO active).

Miller Clamp (Si8285 Only)

SiC FET or IGBT power circuits are commonly connected in a half bridge configuration with the collector of the bottom IGBT tied to the emitter of the top IGBT, or, in the case of SiC FETs, to the drain and source, respectively.

As an example using IGBTs, when the upper switch turns on (while the bottom switch is in the off state), the voltage on the collector of the bottom switch flies up several hundred volts quickly (fast dV/dt). This fast dV/dt induces a current across the IGBT collector-to-gate capacitance (C_{CG}) that constitutes a positive gate voltage spike and can turn on the bottom IGBT. This behavior is called Miller parasitic turn on and can be destructive to the switch since it causes shoot-through current from the positive power rail across the two switches to ground. The Si828x Miller clamp’s purpose is to clamp the gate of the switch device being driven by the Si828x to prevent switch turn on due to the collector C_{CG} coupling. SiC FET half bridge behavior is similar and the Miller clamp's purpose similar, with the effect due to the SiC FET's drain-to-gate capacitance (C_{DG}).

3. Applications Information

The following sections detail the input and output circuits necessary for proper operation. Diagrams display IGBTs for the application examples, but the application circuits are similar for SiC FETs.

For complete application information, please refer to AN1009: Driving MOSFET and IGBT Switches Using the Si828x and AN1306: Driving SiC FETs Using the Si828x Isolated Gate Driver.

3.1 Recommended Application Circuits

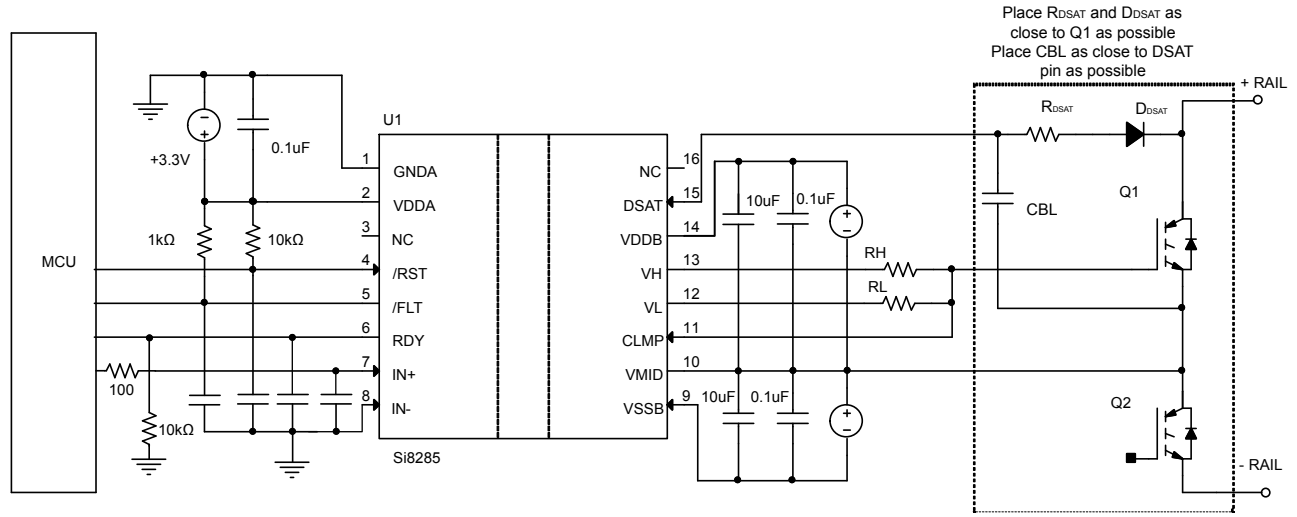


Figure 3.1. Example Si8285 Application Circuit

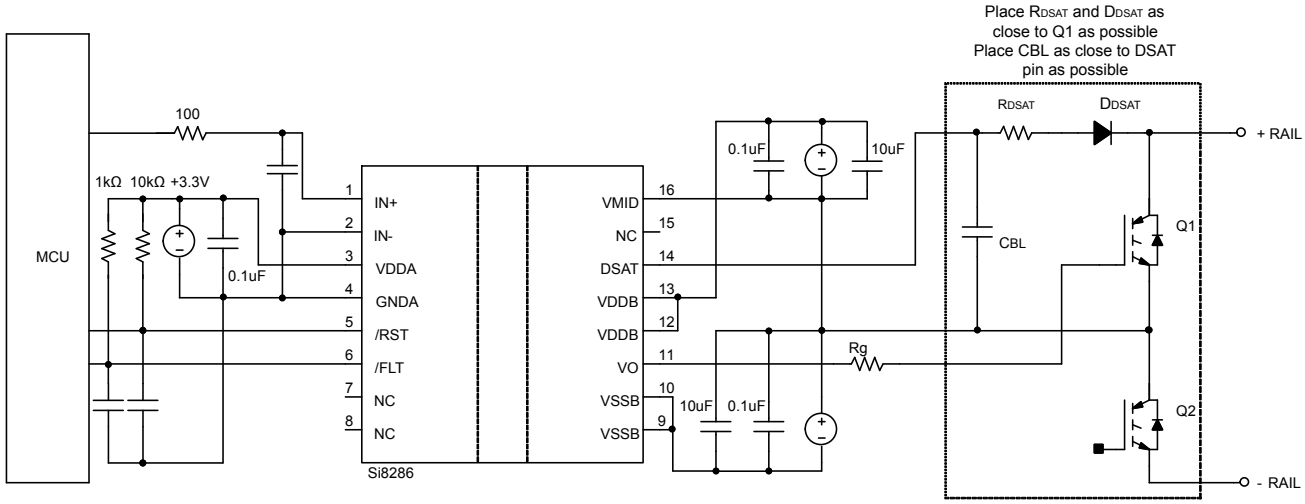


Figure 3.2. Example Si8286 Application Circuit

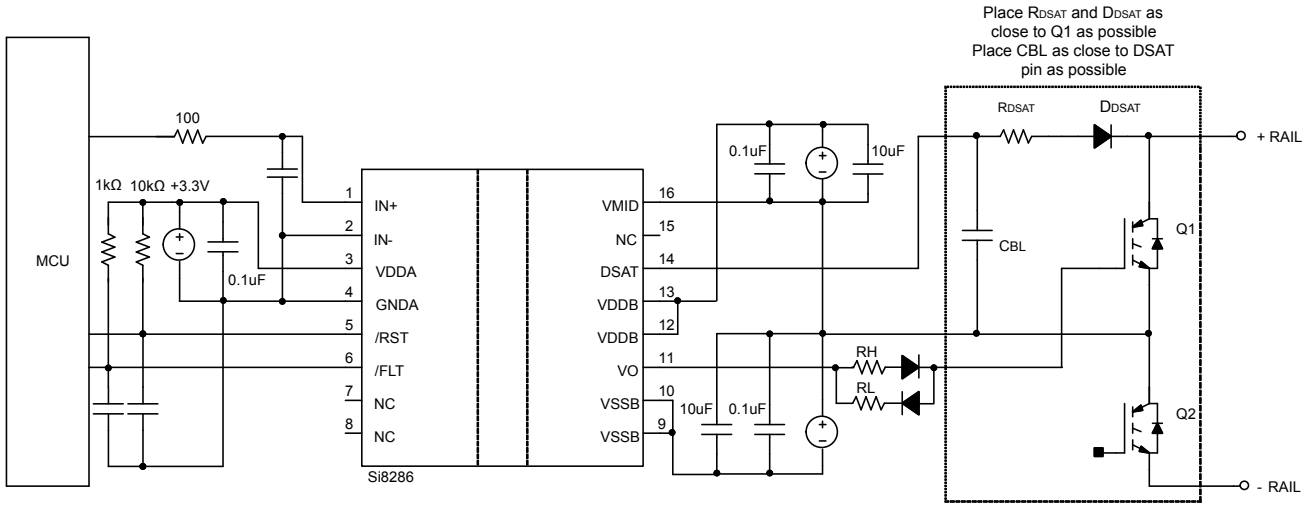


Figure 3.3. Example Si8286 Application Circuit with RH and RL

3.1.1 Power

To power the Si828x, the supply for VDDA should be able to source 10 mA of current. The VDDB and VSSB supplies have to be able to source the Si828x biasing current plus the average switch gate current drive. Each supply should have 0.1 µF and 10 µF parallel bypass capacitors. As shown in Figures 3.1 to 3.3, a supply can be connected between VSSB and VMID to provide a negative bias to the gate drive output, if desired. Such negative gate biases may help reduce switching losses. The VSSB pin should be shorted to VMID if a negative gate bias is not utilized.

3.1.2 Inputs

The Si828x has both inverting and non-inverting gate control inputs (IN– and IN+). In some topologies, one of the inputs is not used and should be connected to GNDA (IN–) or VDDA (IN+) for proper logic termination. Tying IN+ to VDDA allows active-low control of output with IN- pin. Inputs should be driven by CMOS level drivers. It is recommended that the MCU or input driver be located as close to the Si828x as possible to minimize PCB trace parasitics and noise coupling to the input circuit. In noisy environments, it is recommended that one add a small series resistor and an approximately 56pF decoupling cap to the IN traces to attenuate glitches from electrical noise and improve input-to-output signal integrity. The resistor and capacitor values should be large enough to minimize noise but not so large that it affects PWM signals significantly.

The implementation of a differential interface circuit between the MCU and driver's input can greatly improve the noise immunity performance and prevent faulty turn on during high current switching operation.

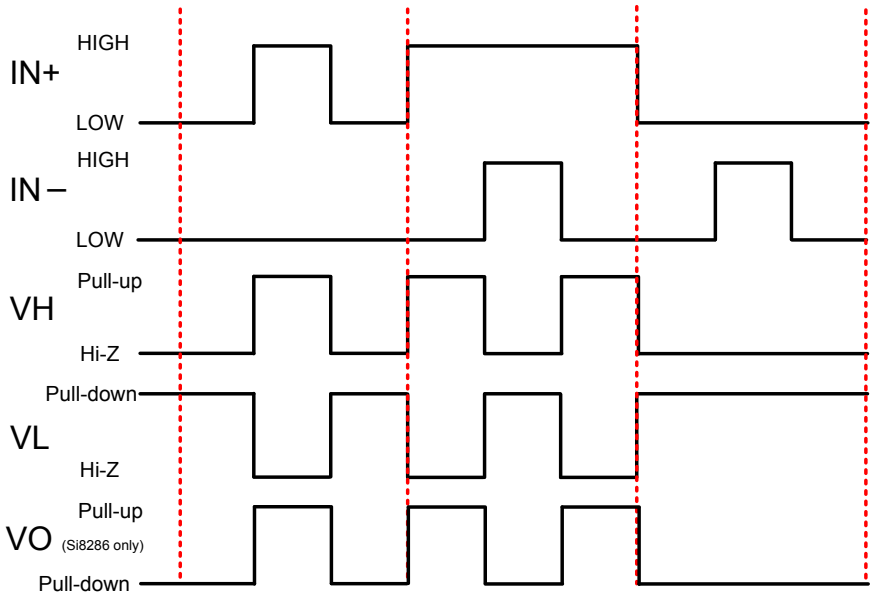


Figure 3.4. Si828x Complementary Input Diagram

3.1.3 Reset, RDY, and Fault

The Si8285 has an active high ready (RDY) push-pull output and needs a 10 kΩ pulldown resistor to prevent false ready indications during power up. On both the Si8285 and Si8286, the open drain fault (FLTb) output needs a pullup resistor (1 kΩ recommended) to prevent false fault indication in noisy environments; furthermore, the active low reset input (RSTb) needs a 10 kΩ pullup to help avoid false resets, particularly at startup.. Fast common-mode transients in high-power circuits can inject noise and glitches into these pins due to parasitic coupling. Depending on the SiC FET or IGBT power circuit layout, additional capacitance (100 pF to 470 pF) can be included on these pins to prevent false RDY and FLTb indications as well as to prevent unintended RSTb reset of the device.

The FLTb outputs from multiple Si828x devices can be connected in an OR wiring configuration to provide a single FLTb signal to the MCU.

The Si828x gate driver will shut down when a fault is detected. It then provides FLTb indication to the MCU and remains in the shutdown state until the MCU applies a reset signal to RSTb.

3.1.4 Desaturation

The Si828x provides sufficient voltage and current to drive and keep the IGBT or SiC FET in saturation during on time to minimize power dissipation and maintain high-efficiency operation. However, abnormal load conditions can force the switch out of saturation and cause permanent damage.

The figure below illustrates the Si828x desaturation circuit. When the Si828x driver output is high, the internal current source is on, and this current flows from the DSAT pin to charge the CBL capacitor. The voltage on the DSAT pin is monitored by an internal comparator. Since the DSAT pin is connected to the SiC FET drain or IGBT collector through the D_{DSAT} and a small R_{DSAT}, its voltage is almost the same as the V_{CE} of the IGBT or V_{DS} of the SiC FET. If this V_{CE} or V_{DS} voltage does not drop below the Si828x desaturation threshold voltage within a certain time after turning on the SiC FET or IGBT (blanking period) the block will generate a fault signal. The Si828x desaturation hysteresis is fixed at 220 mV and threshold is nominally 7 V.

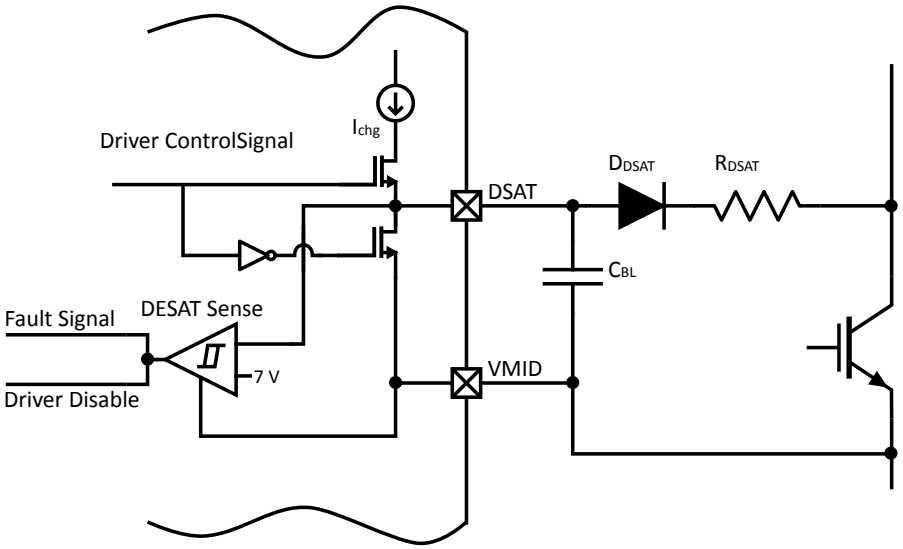


Figure 3.5. Desaturation Circuit (IGBT Example Shown)

As an additional feature, the Si828x supports a blanking timer function to mask the turn-on transient of the external switching device and avoid unexpected fault signal generation. This function requires an external blanking capacitor, C_{BL}, between DSAT and VMID pins. The Si828x includes a current source (I_{Chg}) to charge the C_{BL}. This current source, the value of the external C_{BL}, and the programmed fault threshold, determine the blanking time ($t_{Blanking}$).

$$t_{Blanking} = C_{BI} \times \frac{V_{DESAT}}{I_{chg}}$$

An internal NMOS switch is implemented between DSAT and VMID to discharge the external blanking capacitor, C_{BL}, and reset the blanking timer. The current limiting R_{DSAT} resistor protects the DSAT pin from large current flow toward the SiC FET drain or IGBT collector during the switch's body diode freewheeling period (in some systems it is possible that the IGBT collector voltage drops below VMID, causing current to flow in DSAT).

The desaturation sensing circuit consists of the blanking capacitor (minimum100 pF for Si8286 and 220 pF for Si8285), 100 Ω current limiting resistor, and DSAT diode. These components provide current and voltage protection for the Si828x desaturation (DSAT) pin. It is critical to place the resistor and diode as close to the switch as possible and the capacitor as close to the DSAT pin as possible. On the layout, ensure that the loop formed between these components and the switch is minimized for optimal desaturation detection.

High-frequency oscillation can occur at the driver's output when the following conditions are met: (1) input signals set driver's output to high state, (2) the voltage across the switching device is constantly above VDESAT, and (3) the RSTb is held low. The oscillation is due to the continuous and simultaneous DESAT detection and reset cycles. The oscillation frequency in this DESAT/Reset cycle is in the MHz range and can heat up and damage the Si828x.

To avoid this condition, it is recommended to implement the following DESAT fault reset sequence:

1. Fault detected (FLTb goes low).
2. Set inputs to achieve low output state.
3. Bring RSTb low (minimum 350 ns) to clear the DESAT fault. Refer to Figure 4.5 Device Reaction to Desaturation Event on page 16.
4. Verify fault cleared (FLTb high).
5. Run diagnostic to identify system fault condition
6. Resume operation when it is safe.

3.1.4.1 Soft Shutdown

When soft shut down is activated, the high-power driver goes inactive, and a weak pull-down via VH and external RH discharges the gate until the gate voltage level is reduced to the VSSB + 2 V level. The high power driver is then turned on to clamp the SiC FET or IGBT gate voltage to VSSB.

After the soft shut down, the Si828x driver output voltage is clamped low to keep the SiC FET or IGBT in the off state.

3.1.5 Driver Outputs

The Si8285 has VH and VL gate drive outputs (see Figure 3.1 Example Si8285 Application Circuit on page 7). They work with external RH and RL resistors to limit output gate current. The value of these resistors can be adjusted to independently control SiC FET drain or IGBT collector voltage rise and fall time. The Si8286 only has one VO gate drive output with an external gate resistor to control SiC FET drain or IGBT collector voltage rise and fall time (see Figure 3.2 Example Si8286 Application Circuit on page 7). To achieve independent rise and fall time control, it is suggested to add a pair of fast diodes to the Si8286 VO circuit (see Figure 3.3 Example Si8286 Application Circuit with RH and RL on page 8).

The CLMP output should be connected to the gate of the SiC FET or IGBT directly to provide clamping action between the gate and VSSB pin. This clamping action dissipates the switch's Miller effect current to secure the switch in the off-state. Negative VSSB provides further help to ensure the gate voltage stays below the switch's Vth during the off state.

3.1.6 Miller Clamp (Si8285 Only)

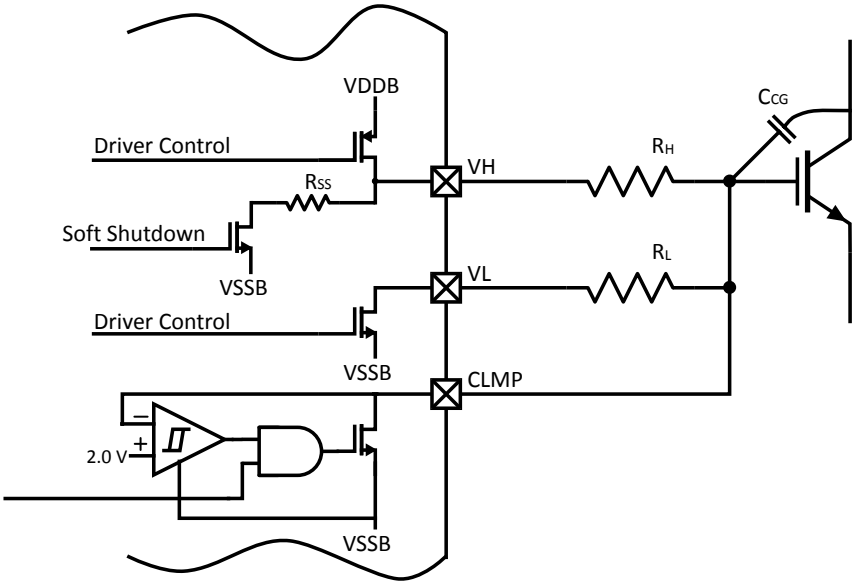


Figure 3.6. Miller Clamp Device (IGBT Example Shown)

The Miller clamp device is engaged after the main driver has been on (VL) and pulled the SiC FET or IGBT gate voltage close to VSSB, such that one can consider the switch being already off. This timing prevents the Miller clamp from interfering with the driver's operation. The engaging of the Miller Clamp is done by comparing the switch gate voltage with a 2.0 V reference (relative to VSSB) before turning on the Miller clamp NMOS.

3.1.7 Additional Adjustments for the Si8285 and Si8286

Additional adjustments of the desaturation detection, soft shutdown, gate current drive, and Miller clamp are possible using external components. Please refer to AN1288: Si828x External Enhancement Circuits for further information.

3.2 Layout Considerations

It is most important to minimize ringing in the drive path and noise on the supply lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si828x as close as possible to the device it is driving. In addition, the supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and power planes for power devices and small signal components provides the best overall noise performance.

4. Electrical Specifications

Table 4.1. Electrical Specifications

V_{DDA} = 3.0 V – 5.5 V (See Figure 3.1 for Si8285, Figure 3.2 for Si8286); Driver supply voltage = V_{DDB}-V_{SSB}, T_A = –40 to +125 °C unless otherwise noted. Minimum value of decoupling capacitors between VDDB and VMID and between VMID and VSSB is 1 µF.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
DC Parameters						
Input Supply Voltage	VDDA		3.0	—	5.5	V
Driver Supply Voltage	(VDDB – VSSB)	Si828xBx	10.0	—	30	V
		Si828xCx	13.2	—	30	V
		Si828xDx	14.0	—	30	V
		Si828xEx	16.0	—	30	V
	(VMID – VSSB)		0	—	15	V
Input Supply Quiescent Current	IDDA(Q)		—	2.6	3.7	mA
Input Supply Active Current	IDDA	f = 10 kHz	—	5.2	—	mA
Output Supply Quiescent Current (Si8285)	IDDB(Q)	Supply voltage = Maximum, No load	—	5.3	6.5	mA
Output Supply Quiescent Current (Si8286)		Supply voltage = Maximum, No load	—	3.5	4.5	mA
Drive Parameters						
High Drive Transistor RDS(ON)	R_{OH}		—	2.48	—	Ω
Low Drive Transistor RDS(ON)	R_{OL}		—	0.86	—	Ω
Internal Soft Shutdown Impedance	R_{SS}			60		Ω
High Drive Peak Output Current[1, 2]	I_{OH}	VDDB = 15 V	2.0	2.7	—	A
Low Drive Peak Output Current[1, 2]	I_{OL}	VSSB = -4 V CL = 220 nF Pulse = 3 µs	4.1	5.5	—	A
UVLO Parameters						
UVLO Threshold +	$VDDA_{UV+}$		2.4	2.7	3.0	
UVLO Threshold –	$VDDA_{UV-}$		2.3	2.6	2.9	
UVLO Lockout Hysteresis– (Input Side)	$VDDA_{HYS}$		—	100	—	mV
UVLO Threshold + (Driver Side) 9 V Threshold (Si828xB) 12 V Threshold (Si828xC) 13 V Threshold (Si828xD) 15 V Threshold (Si828xE)	$VDDB_{UV+}$	$VDDB_{UV+}$ is VDDB referenced to VMID	 8.0 10.8 11.6 13.6	 9.0 12.0 12.8 14.8	 10.0 13.2 14.0 16.0	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
UVLO Threshold – (Driver Side) 9 V Threshold (Si828xB) 12 V Threshold (Si828xC) 13 V Threshold (Si828xD) 15 V Threshold (Si828xE)	$VDDB_{UV-}$	$VDDB_{UV-}$ is VDDB referenced to VMID	 7.0 9.8 10.8 12.8	 8.0 11.0 12.0 14.0	 9.0 12.2 13.2 15.2	V
UVLO Lockout Hysteresis (Driver Side) 9 V/12 V Thresholds (Si828xB/Si828xC) 13 V/15 V Thresholds (Si828xD/ Si828xE)	$VDDB_{HYS}$		—	1 0.75	—	V
UVLO+ to RDY High Delay	$t_{UVLO+ to RDY}$		—		100	µs
UVLO+ to V_X Active Delay	$t_{UVLO+ to Vx\_Active}$				100	µs
ULVO– to RDY Low Delay	$t_{UVLO– to RDY}$		—		0.79	µs
UVLO- to Output OFF Delay	$t_{UVLO- to Output\_OFF}$				0.79	µs
Desaturation Detector Parameters						
DESAT Threshold	VDESAT	VDDB – VSSB > VDDBUV+	6.25	6.9	7.4	V
C_{BI} charging current (Si8285)	I_{Chg}		—	1	—	mA
C_{BI} charging current (Si8286)			—	0.25	—	mA
DESAT Sense to 90% VH (VO for Si8286) Delay	$t_{DESAT(90\%)}$	RH = RL = Rg = 10 Ω CL = 10 nF	—	270	350	ns
DESAT Sense to 10% VH (VO for Si8286) Delay	$t_{DESAT(10\%)}$	RH = RL = Rg = 10 Ω CL = 10 nF	—	1.8	2.3	µs
DESAT Sense to FLTb Low Delay	$t_{DESAT to FLTb}$		—	220	300	ns
Reset to FLTb High Delay	$t_{RSTb to FLTb}$		—	270	350	ns
Reset Pulse Width	t_{RSTb}		350	—	—	ns
Miller Clamp Parameters (Si8285 Only)						
Clamp Pin Threshold Voltage	V_t Clamp		—	2.0	—	V
Miller Clamp Transistor RDS (ON)	R_{MC}		—	1.07	—	Ω
Clamp Low Level Sinking Current[1, 2]	I_{CL}	VCLMP = VSSB + 6.0	3.0	3.4	—	A
Digital Parameters						
Logic High Input Threshold	VIH		2.0	—	—	V
Logic Low Input Threshold	VIL		—	—	0.8	V
Input Hysteresis	VIHYST		—	440	—	mV
High Level Output Voltage (RDY pin only)	VOH	IO = –4 mA	VDDA – 0.4	—	—	V
Low Level Output Voltage (RDY pin only)	VOL	IO = 4 mA	—	—	0.4	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Open-Drain Low Level Output Voltage (FLTb pin only)		VDDA = 5 V, 5 kΩ pull-up resistor	—	—	200	mV
AC Switching Parameters						
Propagation Delay (Low-to-High)	t_{PLH}	CL = 200 pF	30	40	50	ns
Propagation Delay (High-to-Low)	t_{PHL}	CL = 200 pF	30	40	50	ns
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$ for a single device	—	1	5	ns
Propagation Delay Difference[2]	PDD	$t_{PHLMAX} - t_{PLHMIN}$	–1	—	25	ns
Rise Time[2] (10% to 90%)	t_R	CL = 200 pF	—	5.5	15	ns
Fall Time[2] (90% to 10%)	t_F	CL = 200 pF	—	8.5	20	ns
Common Mode Transient Immunity		Output = low or high (VCM = 1500 V)	125	—	—	kV/µs

1. When performing this test, it is recommended that the DUT be soldered to avoid socket and trace inductances, which may cause overstress conditions.
2. Guaranteed by characterization.

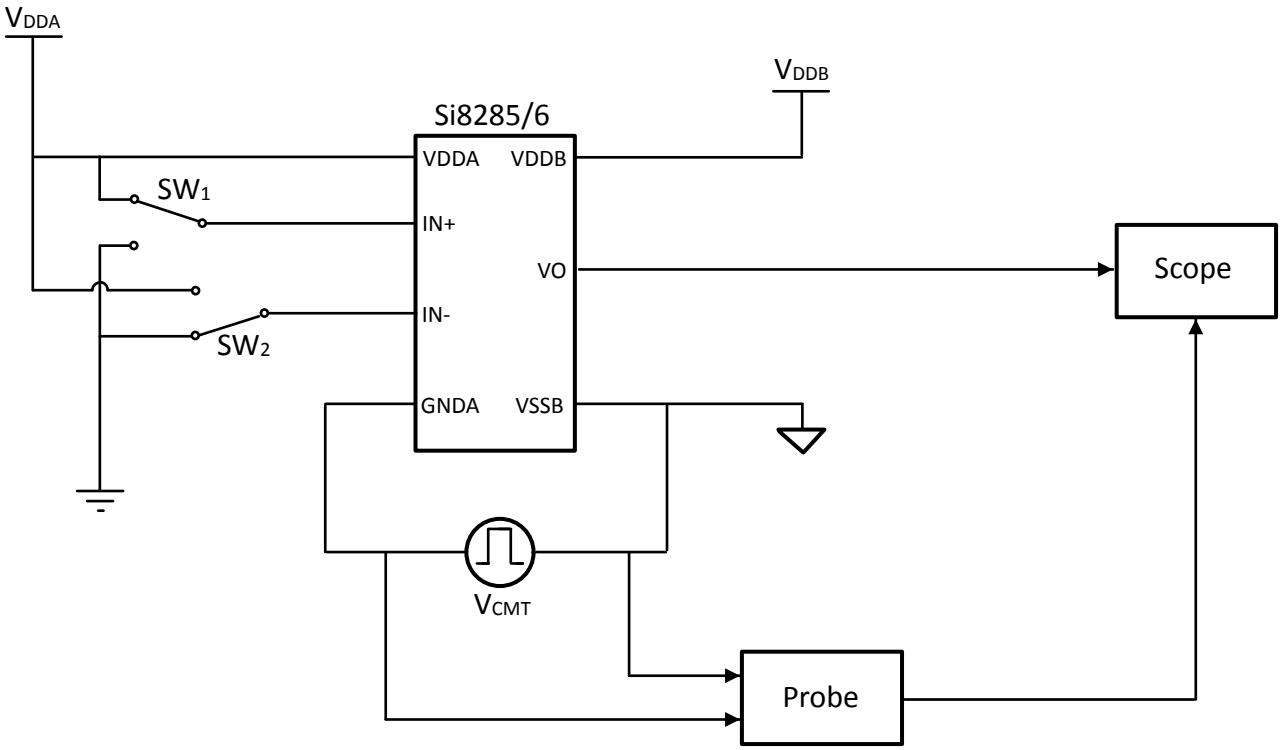


Figure 4.1. Common-Mode Transient Immunity Characterization Circuit

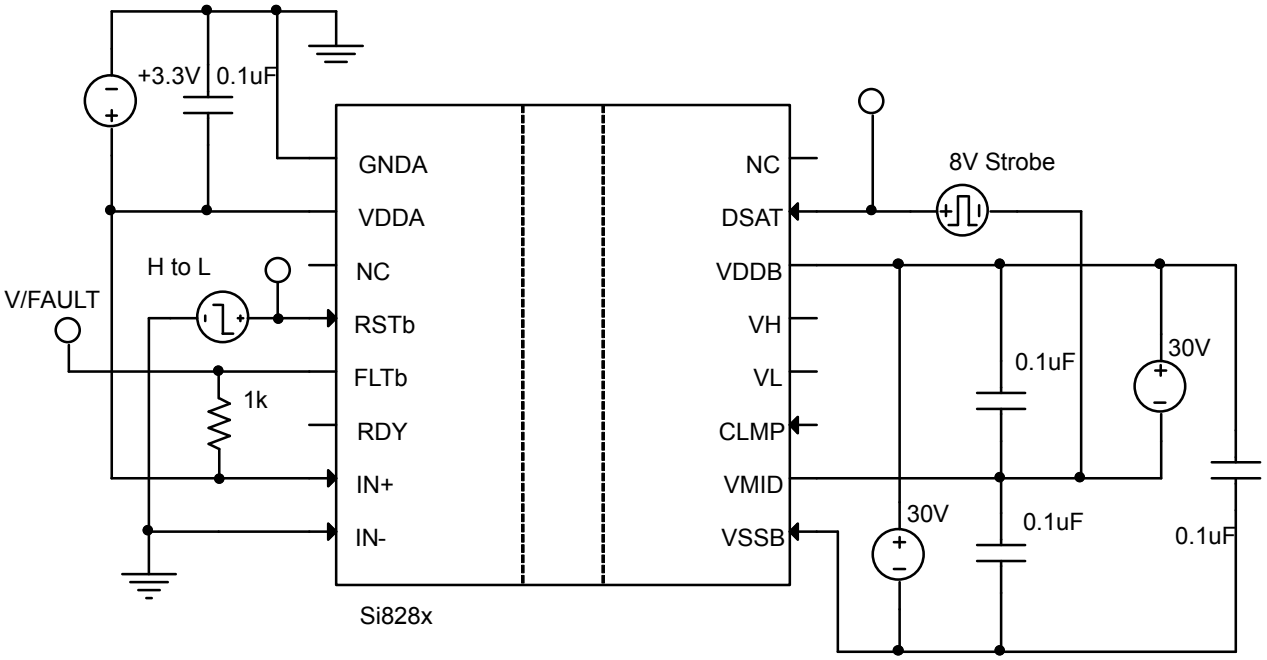


Figure 4.2. Si828x RSTb FLTb CLEAR Test Circuit

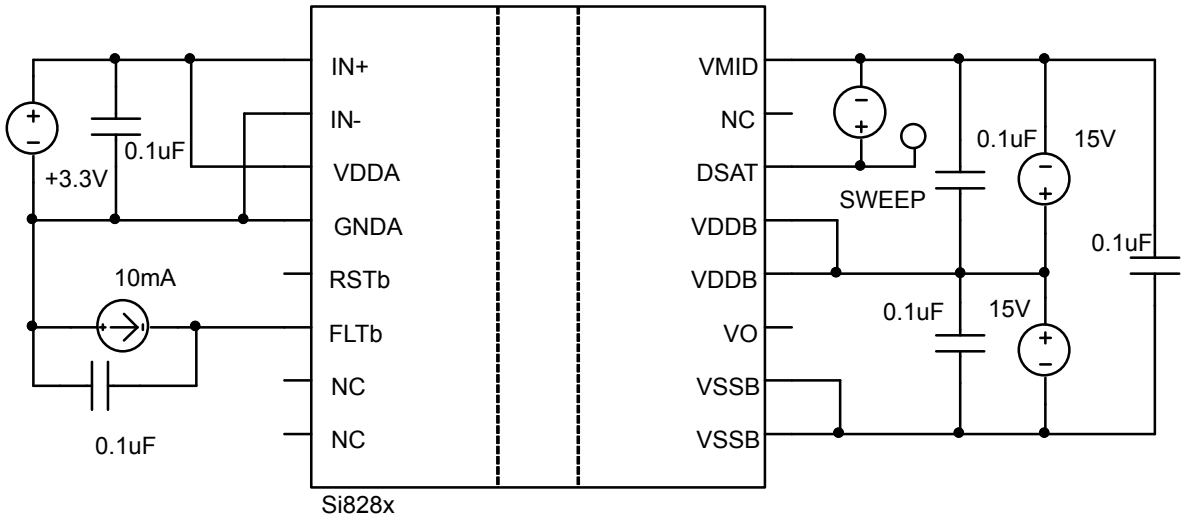


Figure 4.3. Si828x DSAT Threshold Test Circuit

Table 4.2. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	–65	+150	°C
Operating Temperature	T_A	–40	+125	°C
Junction Temperature	T_J	—	+140	°C
Peak Output Current (t_{PW} = 10 µs)	I_{OPK}	—	4.0	A
Input Side Supply Voltage	VDDA - GNDA	-0.5	6	V
Output Side Supply Voltage	VDDB - VSSB	–0.5	36	V
Output Voltage	VH/VL/VO	–0.5	36	V

Parameter	Symbol	Min	Max	Unit
Input Power Dissipation	P_I	—	100	mW
Output Power Dissipation	P_O	—	800	mW
Total Power Dissipation (All Packages Limited by Thermal Derating Curve)	P_T	—	900	mW
Lead Solder Temperature (10 s)		—	260	°C

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.1 Timing Diagrams

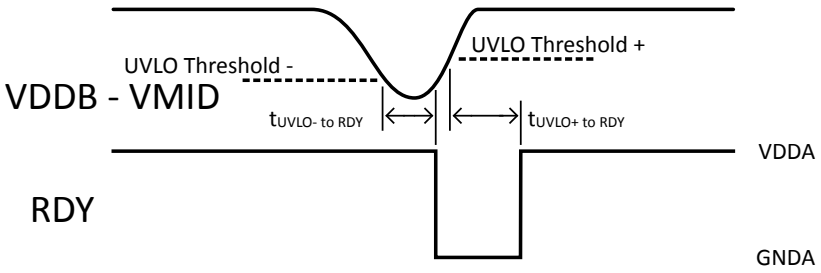


Figure 4.4. UVLO Condition to RDY Output

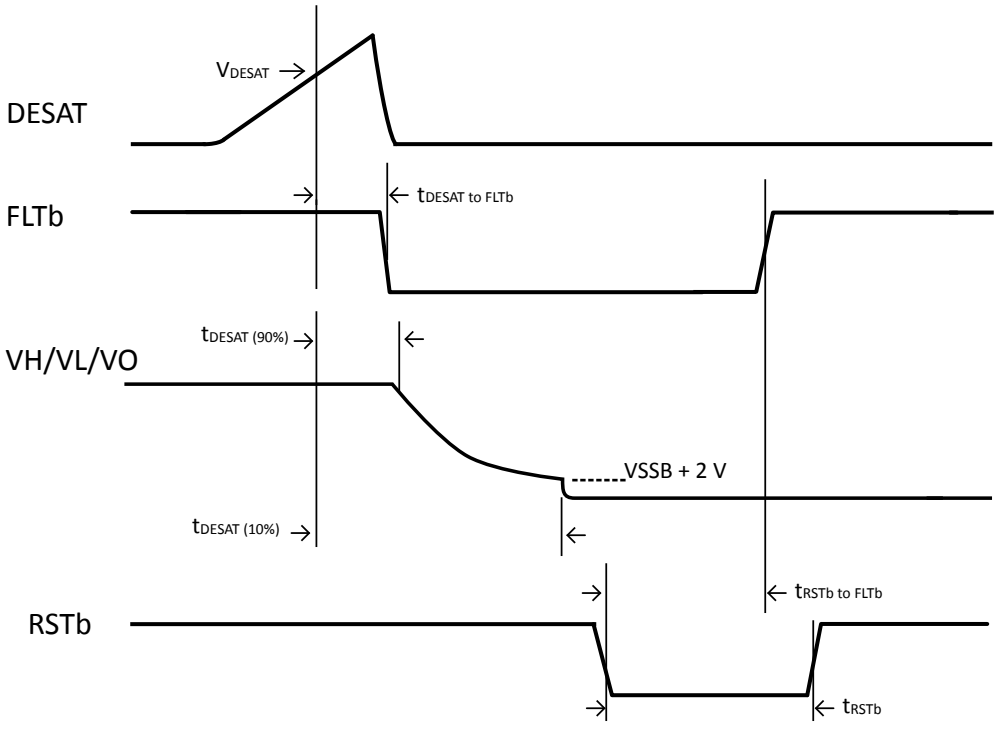
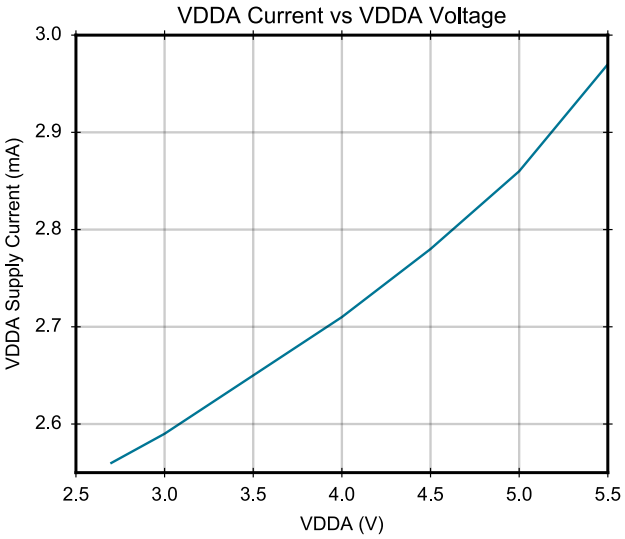
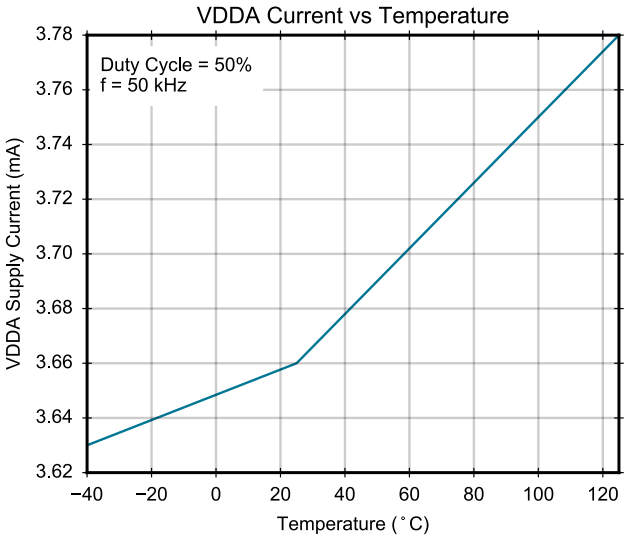


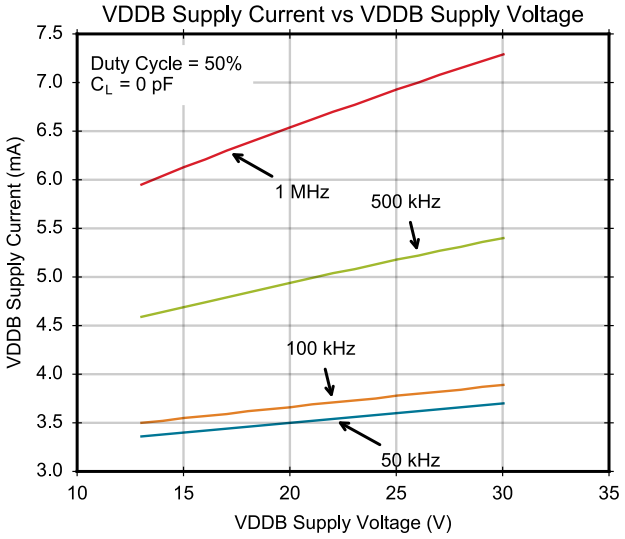
Figure 4.5. Device Reaction to Desaturation Event

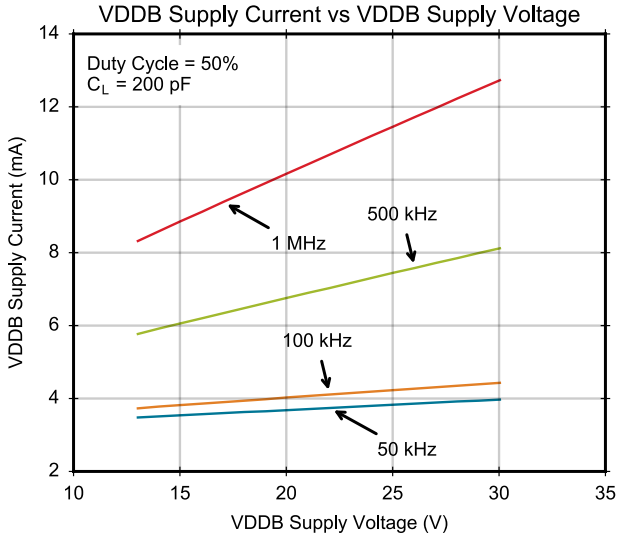
4.2 Typical Operating Characteristics

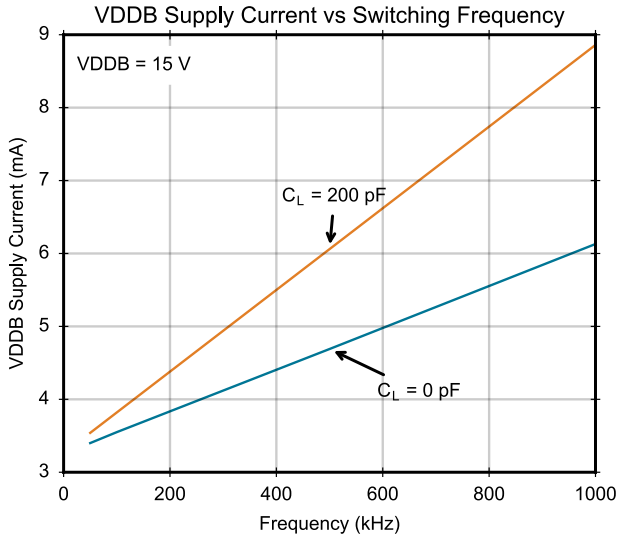
Note: $T_{ambient}$ = 25°C, unless stated otherwise.

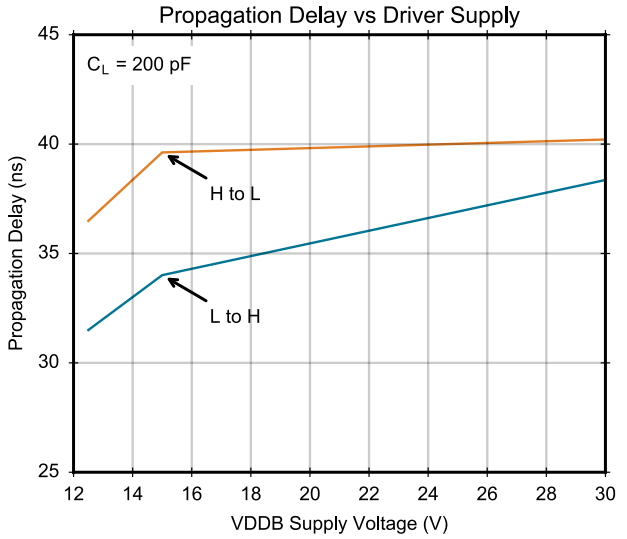


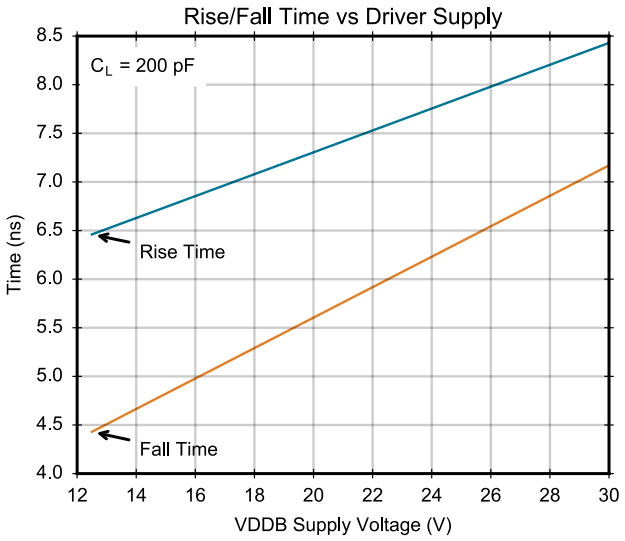


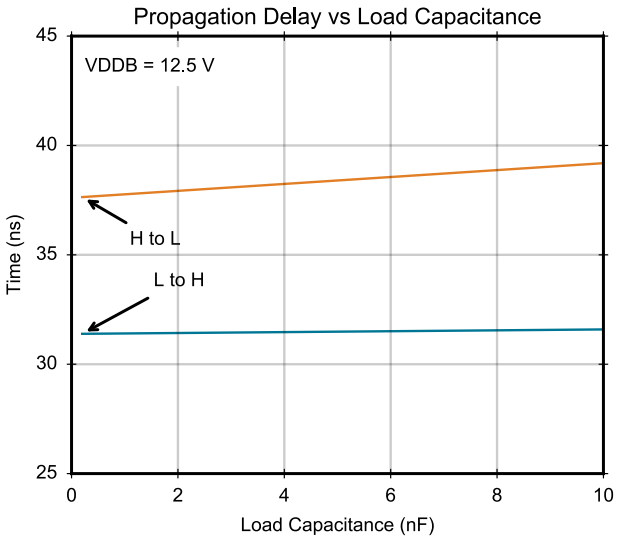


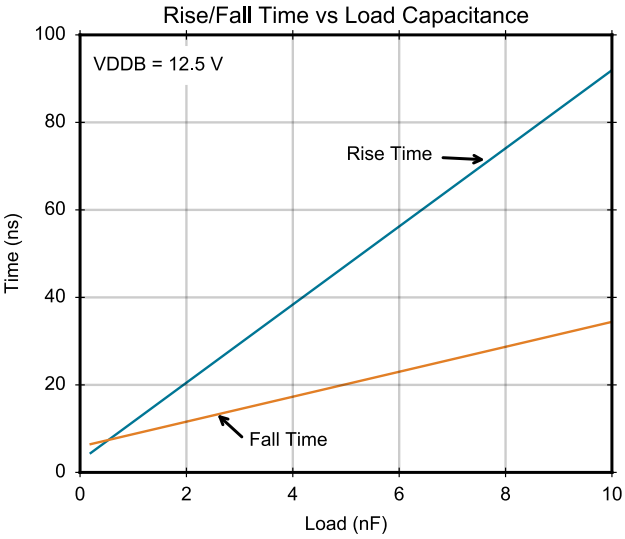


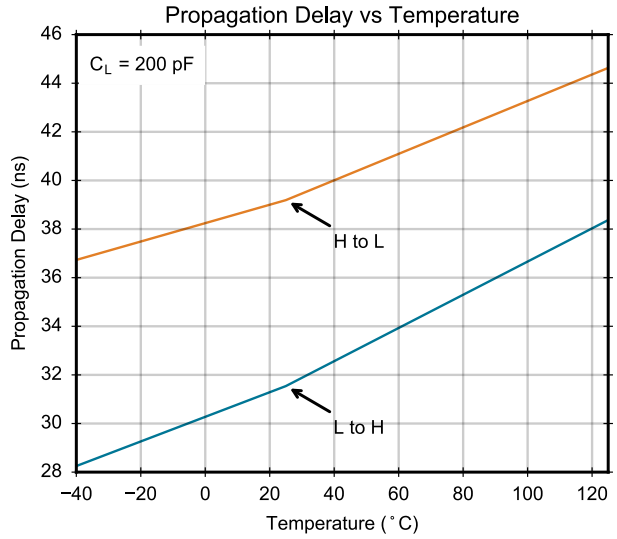


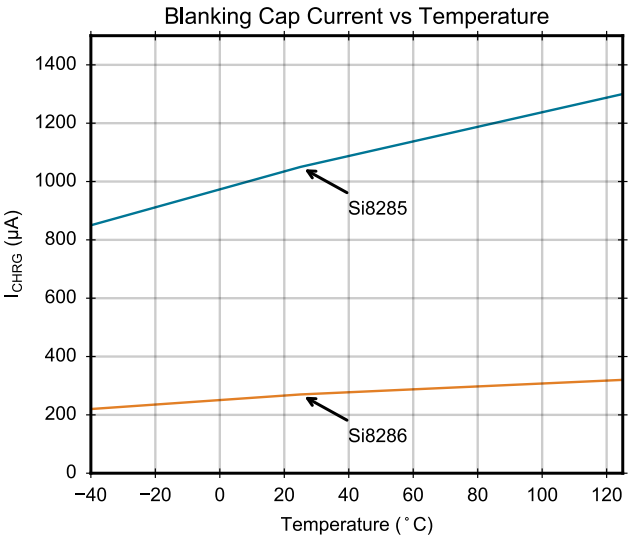


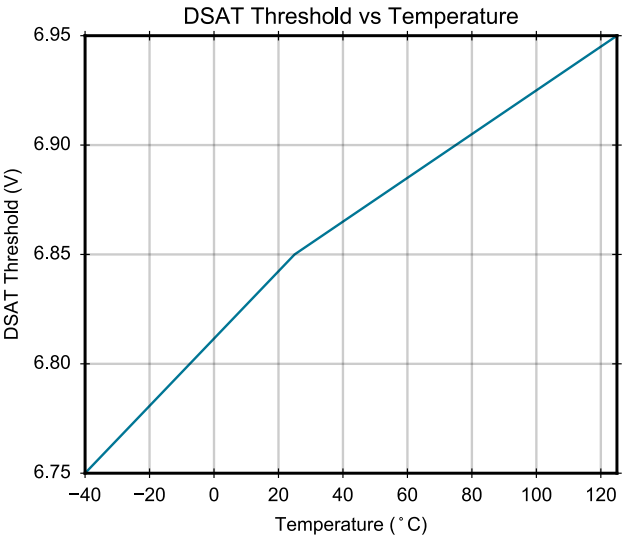

Rise/Fall Time vs Driver Supply
C_L = 200 pF
Rise Time
Fall Time
Time (ns)
VDDB Supply Voltage (V)

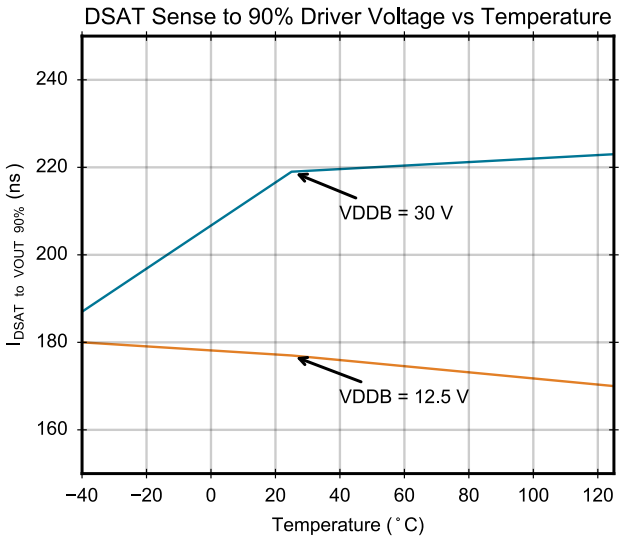

Propagation Delay vs Load Capacitance
VDDB = 12.5 V
H to L
L to H
Time (ns)
Load Capacitance (nF)

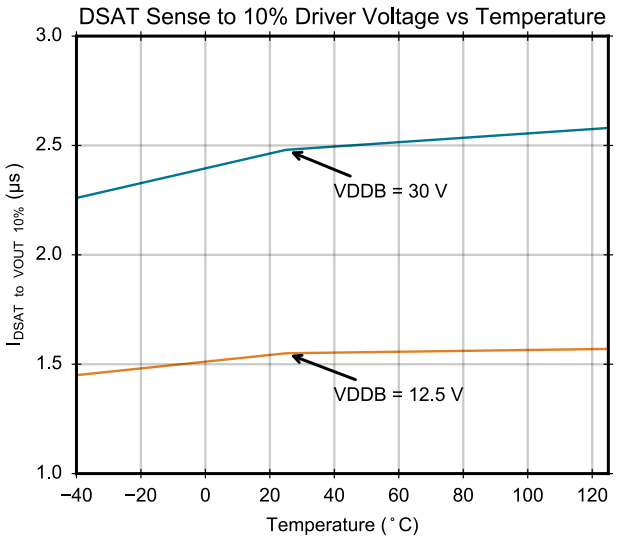

Rise/Fall Time vs Load Capacitance
VDDB = 12.5 V
Rise Time
Fall Time
Time (ns)
Load (nF)

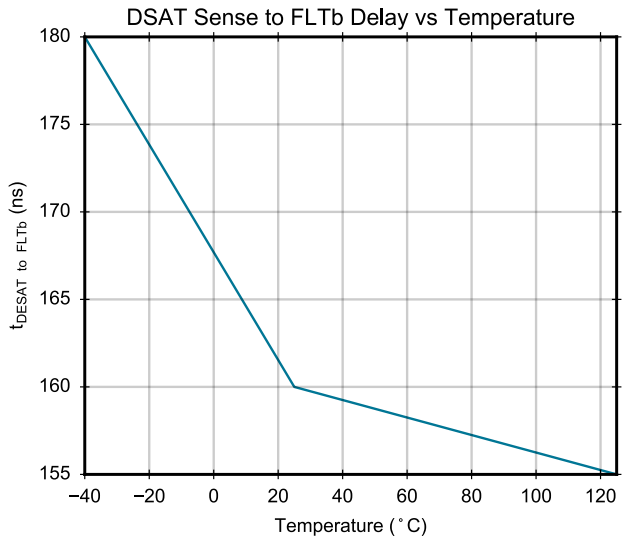

Propagation Delay vs Temperature
C_L = 200 pF
H to L
L to H
Propagation Delay (ns)
Temperature (˚C)


Blanking Cap Current vs Temperature
Si8285
Si8286
I_{CHRG} (µA)
Temperature (˚C)


DSAT Threshold vs Temperature
DSAT Threshold (V)
Temperature (˚C)


DSAT Sense to 90% Driver Voltage vs Temperature
240
220
200
180
160
−40
−20
0
20
40
60
80
100
120
Temperature (˚C)
tDSAT to VOUT 90% (ns)
VDDB = 30 V
VDDB = 12.5 V


DSAT Sense to 10% Driver Voltage vs Temperature
3.0
2.5
2.0
1.5
1.0
−40
−20
0
20
40
60
80
100
120
Temperature (˚C)
tDSAT to VOUT 10% (µs)
VDDB = 30 V
VDDB = 12.5 V


DSAT Sense to FLTb Delay vs Temperature
180
175
170
165
160
155
−40
−20
0
20
40
60
80
100
120
Temperature (˚C)
tDESAT to FLTb (ns)

4.3 Regulatory Information

Table 4.3. Regulatory Information (Pending)[1, 2]

CSA
The Si828x is certified under CSA. For more details, see Master Contract Number 232873.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
VDE
The Si828x is certified according to IEC60747-17. For more details, see File 5006301-4880-0001. IEC60747-17: Up to 1414 V_{PEAK} for basic insulation working voltage.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si828x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage (V_{ISO}) for basic protection.
CQC
The Si828x is certified under GB4943.1-2011.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
Note: 1. Regulatory Certifications apply to 3.75 and 5.0 kV_{RMS} rated devices, which are production tested to 4.5 and 6.0 kV_{RMS} for 1 sec, respectively. 2. For more information, see Section 1. Si8285/86 Ordering Guide.

Table 4.4. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value	Unit
			WB SOIC-16	
Nominal External Air Gap (Clearance)[1]	CLR		8.0	mm
Nominal External Tracking (Creepage)	CRP		8.0	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.016	mm
Tracking Resistance	PTI or CTI	IEC60112	600	V
Erosion Depth	ED		0.019	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	1	pF

Note:
1. The values in this table correspond to the nominal creepage and clearance values as detailed in Section 6.1 Package Outline: 16-Pin Wide Body SOIC. VDE certifies the clearance and creepage limits as 8.5 mm minimum for the WB SOIC-16. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 7.6 mm minimum for the WB SOIC package.
2. To determine resistance and capacitance, the Si828x is converted into a 2-terminal device. All pins on input side are shorted together to form the first terminal, and similarly, all pins on the output side are shorted together to form the second terminal. The parameters are then measured between these two terminals.

Table 4.5. IEC 60664-1 Ratings

Parameter	Test Condition	Specification
		WB SOIC-16
Basic Isolation Group	Material Group	I
Overvoltage Category	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 600 V_{RMS}	I-IV

Table 4.6. IEC60747-17 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic	Unit
			WB SOIC	
Maximum Working Isolation Voltage	V_{IOWM}		1000	V_{RMS}
Maximum Repetitive Isolation Voltage	V_{IORM}		1414	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	2652	V peak
Maximum Transient Isolation Voltage	V_{IOTM}	t = 60 sec	8000	V peak
Maximum Surge Isolation Voltage	V_{IOSM}	Tested with 8000 V_{peak} and 1.2 µs/50 µs profle	6150	V peak
Maximum Impulse Voltage	V_{IMP}	Tested with 6150 V_{peak} and 1.2 µs/50 µs profle	6150	V peak
Pollution Degree		DIN VDE 0110	2	
Insulation Resistance	R_S	T_{AMB} = $T_{S,}$, V_{IO} = 500 V	>10^9	Ω

Note:
1. Maintenance of the safety data is ensured by protective circuits. The Si828x provides a climate classification of 40/125/21.

Table 4.7. IEC60747-17 Safety Limiting Values[1, 2]

Parameter	Symbol	Test Condition	Max	Unit
			WB SOIC-16	
Safety Temperature	T_S		140	°C
Safety Current	I_S	θ_{JA} = 73 °C/W V_{DDA} = 5.5 V, V_{DDB}–V_{SSB} = 30 V T_J = 140 °C, T_A = 25 °C	52.5	mA
Safety Power	P_S		1.575	W

Note:
1. Maximum value allowed in the event of a failure.
2. See Figure 4.6 for Thermal Derating Curve.

Table 4.8. Thermal Characteristics

Parameter	Symbol	Typ	Unit
		WB SOIC-16	
IC Junction-to-Air Thermal Resistance	θ_{JA}	73	°C/W

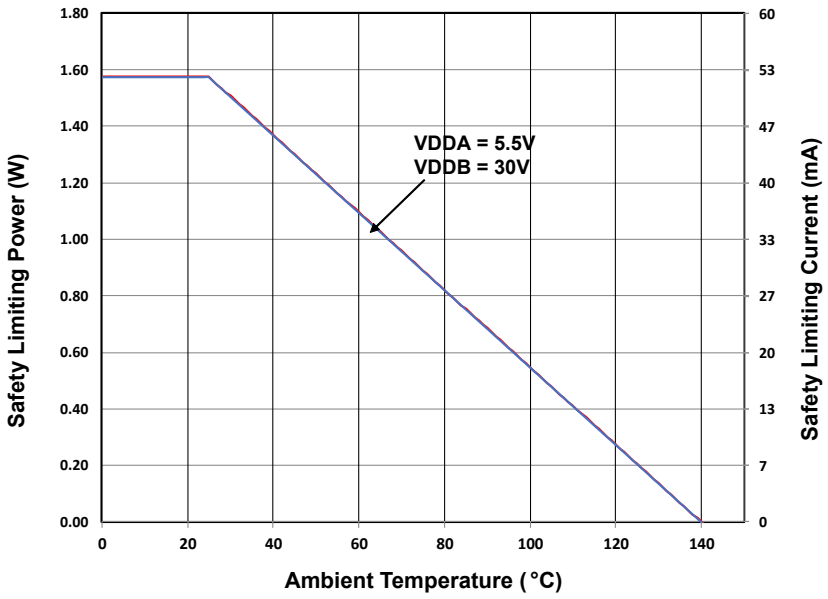
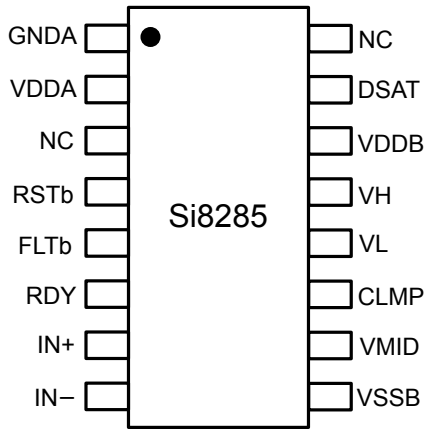


Figure 4.6. WB SOIC-16 Thermal Derating Curve

5. Pin Descriptions



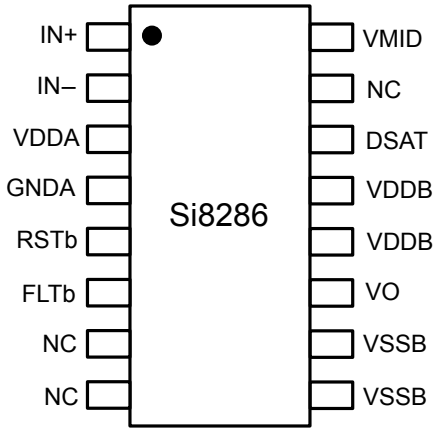


Table 5.1. Si8285/86 Pin Descriptions

Name	Si8285 Pin #	Si8286 Pin #	Description
GNDA	1	4	Input side ground
VDDA	2	3	Input side power supply
RSTb	4	5	Reset fault condition pin
FLTb	5	6	Driver fault condition signal
RDY	6	—	UVLO ready signal
IN+	7	1	Driver control complementary input (+)
IN–	8	2	Driver control complementary input (–)
VSSB	9	9, 10	Driver output side ground
VMID	10	16	IGBT source reference
CLMP	11	—	Miller clamp drain
VL	12	—	Pull-low driver output
VH	13	—	Pull-high driver output
VO	—	11	Driver output
VDDB	14	12, 13	Driver output power supply
DSAT	15	14	Desaturation detection sensor input
NC[1]	16	7, 8, 15	No Connect

Note:

1. No Connect. These pins may be internally connected. For optimal performance and safety, these pins must be connected to their respective grounds: GNDA for input side and VSSB for output side.

6. Packaging

6.1 Package Outline: 16-Pin Wide Body SOIC

The figure below illustrates the package details for the Si828x in a 16-Pin Wide Body SOIC. The table lists the values for the dimensions shown in the illustration.

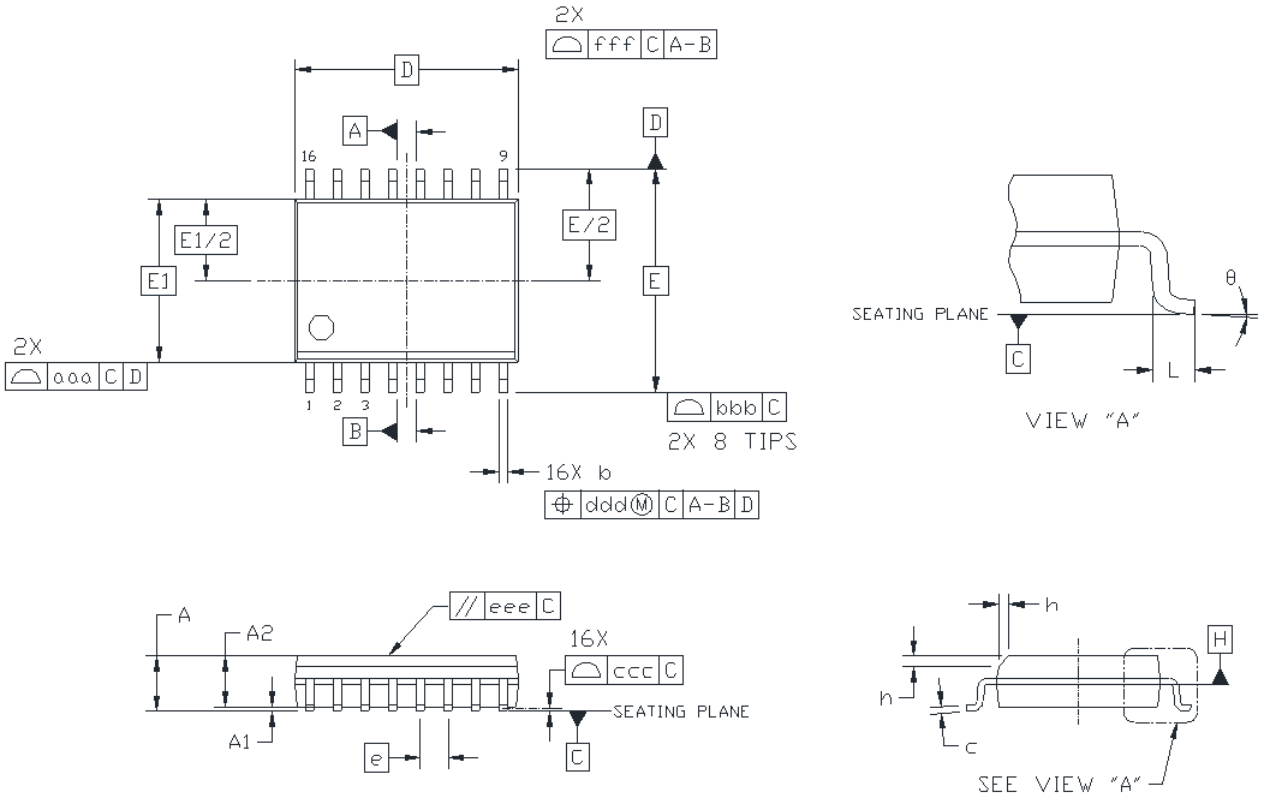


Figure 6.1. 16-Pin Wide Body SOIC

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
aaa	—	0.10
bbb	—	0.33

Symbol	Millimeters	
	Min	Max
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

6.2 Land Pattern: 16-Pin Wide Body SOIC

The figure below illustrates the recommended land pattern details for the Si828x in a 16-Pin Wide Body SOIC. The table lists the values for the dimensions shown in the illustration.

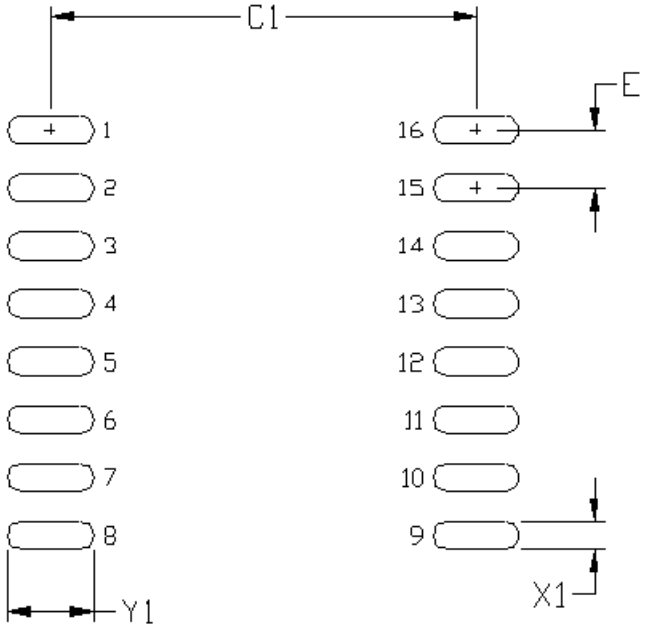


Figure 6.2. PCB Land Pattern: 16-Pin Wide Body SOIC

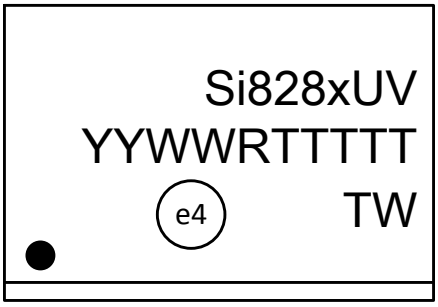
Table 6.1. 16-Pin Wide Body SOIC Land Pattern Dimensions[1, 2]

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Note:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC), and a card fabrication tolerance of 0.05 mm is assumed.

6.3 Top Marking: 16-Pin Wide Body SOIC



Si8285/86 Top Marking

Table 6.2. Si8285/86 Top Marking Explanation

Line 1 Marking:	Customer Part Number	Si8285, Si8286 = Product Configuration U = UVLO level: B = 9 V; C = 12 V; D = 13 V and E = 15 V V = Isolation rating: C = 3.75 kV; D = 5.0 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
	RTTTTT = Mfg Code	Manufacturing code “R” indicates revision
Line 3 Marking:	TW	Country of Origin

7. Revision History

Revision 2.0

April, 2021

- Restructured and updated Product Overview and Applications Information sections
- Updated numerous Electrical specifications in Table 4.1 Electrical Specifications on page 12 and Table 4.2 Absolute Maximum Ratings[1] on page 15
- Clarified timing diagrams in Section 4.1 Timing Diagrams
- Updated Regulatory Information in Table 4.3 Regulatory Information (Pending)[1, 2] on page 20

Revision 1.1

August, 2018

- Corrected typo for minimum VDDA and VDDB in Table 4.1 Electrical Specifications on page 12 to match the max UVLO values stated in the same table.

Revision 1.0

March, 2018

- Updated Safety Regulatory Approvals section on page 1, and Tables 4.3, 4.4, and 4.6 to conform with isolation component standard terminology.
- Removed references to IEC 60747-5-5 throughout the document and replaced with VDE 0884.
- Added automotive (-A) OPNs.
- Updated Thermal Derating Curve, Figure 4.6.

Revision 0.6

November, 2016

- Corrected junction temperature in Table 4.2 Absolute Maximum Ratings[1] on page 15.

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